**module mux21 (I0, I1, Sel, Out);**

**input I0, I1, Sel;**

**output Out;**

**assign Out=(!Sel&I0)|(Sel&I1);**

**endmodule**

**--------------------------------------------------**

**module mux21 (I0, I1, Sel, Out);**

**input I0, I1, Sel;**

**output Out;**

**wire Sel\_bar, w1, w2;**

**not n1 (Sel\_bar, Sel);**

**and a1 (w1, Sel\_bar, I0);**

**and a2 (w2, Sel, I1);**

**or o1 (Out, w1, w2);**

**endmodule**

**--------------------------------------------------**

**module mux21 (I0, I1, Sel, Out);**

**input I0, I1, Sel;**

**output Out;**

**assign Out=Sel?I1:I0;**

**endmodule**

**--------------------------------------------------**

**module mux21 (I0, I1, Sel, Out);**

**input I0, I1, Sel;**

**output Out;**

**always @ (\*)**

**case (Sel)**

**1'b0: Out=I0;**

**1'b1: Out=I1;**

**default: Out=0;**

**endcase**

**endmodule**

**--------------------------------------------------**

**module mux21 (I0, I1, Sel, Out);**

**input I0, I1, Sel;**

**output Out;**

**always @ (\*)**

**if (Sel)**

**Out=I1;**

**else**

**Out=I0;**

**endmodule**

**--------------------------------------------------**

**module mux21 (I0, I1, Sel, Out);**

**input I0, I1, Sel;**

**output Out;**

**always @ (\*)**

**if (Sel==1'b0)**

**Out=I0;**

**else**

**Out=I1;**

**endmodule**

**--------------------------------------------------**